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EXAMINER

RUTLAND WALLIS, MICHAEL

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/812,395

Applicant(s)

EGERER, JENS

Examiner

Michael Rutland-Wallis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>03/30/2004</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 03/30/2004 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

The disclosure is objected to because Applicant's disclosure recites only one heading "Description". Correction is required see 37 CFR 1.77(b). The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in

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upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if

the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

In claim 17 is objected to wherein the limitation "PLDs and/or PLAs" is recited in line 3 of the claim. While for the purposes of examination on the merits said limitation will be treated as "programmable logic devices and programmable logic arrays" please identify the meaning of said acronyms at the first usage/occurrence of the acronym.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language.

The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949).

In the present instance, claim 17 recites the broad recitation fundamental memory devices, and the claim also recites in particular PLDs and/or PLAs, which is the narrower statement of the range/limitation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 10-12, 18-21 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Chu et al. (U.S. Pat. No. 5,508,653)

With respect to claim 1 Chu teaches a system (Fig. 2) comprising first semiconductor device (item 12), and second semiconductor device (item 14b), wherein the first semiconductor device (item 12) comprises a voltage supply means (20b from voltage supply connection item 24), characterized in that said voltage supply means of

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said first semiconductor device is connected (see Fig. 2) to said second semiconductor device (item 14b), so that said voltage supply means of said first semiconductor device can provide a supply voltage for said second semiconductor device.

With respect to claim 2 Chu teaches said first semiconductor device and said second semiconductor device are arranged in the same system (Fig. 2). Chu further teaches the system is used in laptop computers (col. 1 lines 20-25) and laptop computers are contained within housings.

With respect to claim 8 Chu teaches the system comprising one further semiconductor devices (see Fig. 2 showing multiple semiconductors devices 14a for example).

With respect to claim 10 Chu teaches the voltage supply means (24) of said first semiconductor device (12) is additionally also connected to said one further semiconductor device (via low power bus common to devices connected to input 24 in Fig. 2), so that said voltage supply means (20b) of said first semiconductor device can additionally provide a supply voltage for said one or said several further semiconductor device (see series connection of power supplied to buffer 20b associated with semiconductor device 14a).

With respect to claim 11 Chu teaches first semiconductor device (12) comprises a further voltage supply means (26) that is connected to said one semiconductor device, so that said further voltage supply means of said first semiconductor device (12) can provide (via low power bus connecting buffers) a supply voltage for said one semiconductor device (Fig. 2).

With respect to claim 12 Chu teaches the second semiconductor device is a memory device.

With respect to claim 18 Chu teaches the voltage supply means (24) provide a voltage supply for said first semiconductor device (12).

With respect to claim 19 Chu teaches the voltage supply means generates the respective supply voltage from an external voltage (item 15).

With respect to claims 20 and 21 Chu teaches the voltage supply means (24/26) comprise a voltage regulating means (buffer item 20b) and charge pump (via item 22) to control the voltage to memory modules with different voltage requirements.

With respect to claim 27 Chu teaches a device function adjusting means (connection wire bonding and associated buffer circuitry, alternatively see item 22), in particular an appropriate fuse (bonding wire connecting components item Fig. 2), is provided on said first semiconductor device (12), by means of which it is determined whether the corresponding semiconductor device is to assume the function of said first semiconductor device.

With respect to claim 28 Chu teaches the voltage supply means (24) of said first semiconductor device (12) is connected to a corresponding pad (see in Fig. 2) of said first semiconductor device (12).

With respect to claim 29 Chu teaches the pad of said first semiconductor device is connected to a corresponding pad of said second semiconductor device, which said voltage supply means of said second semiconductor device can be connected to (see Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-7, 9, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (U.S. Pat. No. 5,508,653) in view of Applicant's admitted prior art.

With respect to claims 4-7 Chu is silent on the on the detailed nature of the components and whether said components are plug mountable, DIL, SMD or PGA. As Applicant admits to on page 2 lines 24-31 discloses semiconductors are usually incorporated in appropriate housings e.g. SMD, plug mountable, DIL, PGA etc... It would have been obvious to one of ordinary skill in the art at the time of the invention to connected semiconductors as appropriate to the housing in order to provide a simple and reliable connection to other connected semiconductors.

With respect to claim 9 Chu teaches said one further semiconductor device is arranged in the same system, as the first and said second semiconductor devices (12 and 14b). Chu does not teach the circuitry is contained within a housing, semiconductor components are typically found a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the system of Chu into

a housing if in fact such a housing is not utilized by Chu in order to protect the semiconductor.

With respect to claim 30 Chu teaches the pad of said first semiconductor device is connected directly (though buffer) to the corresponding pad of said second semiconductor device by means of an appropriate bonding wire (see Fig. 2).

With respect to claim 31 Chu teaches the pad of said first semiconductor device is connected indirectly to the corresponding pad of said second semiconductor device. Chu does not teach the use of an interposer, however the interconnection seen in Fig. 1 between circuit blocks. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an interposer or other connection means to connect the circuit blocks in order to provide a reliable connection between circuit blocks.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (U.S. Pat. No. 5,508,653) in view of Proebstring (U.S. Pat. No. 5,687,108) Chu teaches the first and second semiconductor devices are arranged in the same system and is used for memory devices. The arrangement of memory arrays is typically configured in a stacked manner. Proebstring teaches an arrangement of memory arrays in a stacked manner. It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange the connection of semiconductor devices in a stacked manner in order to utilize the space efficiently.

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa et al. (U.S. Pub. No. 2004/0094820) in view of Odisho et al. (U.S. Pat. No. 5,758,100)

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With respect to claim 13-14 Chu is silent on the on the detailed nature of the components specifically the type of memory device. Odisho teaches a typical semiconductor integrated circuit (item 202) comprising a memory device (RAM module item 212). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semiconductor voltage supply configuration of Chu with memory devices as seen in Odisho in order to supply memory modules with variable voltage requirements.

With respect to claim 15 Chu as modified by Odisho are silent on whether the RAM is DRAM (dynamic RAM) as understood by the examiner the RAM modules are DRAM modules, while not explicitly stated by Odisho, however should one contend otherwise, It would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM modules in order to supply typical memory modules is a computer with voltage.

With respect to claim 16 Odisho teaches the memory devices items 212 and additional circuitry may comprise a graphics card or a network card (col. 2 line 55) known to one of ordinary skill in the art to utilize ROM.

With respect to claim 17 Chu as modified by Odisho teach said memory device is a functional memory device or fundamental memory devices, respectively, in particular PLDs and/or PLAs as the memory devices of Odisho are controlled by a memory address bus and made up of transistors.

Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. (U.S. Pat. No. 5,508,653) in view of Barber et al. (U.S. Pat. No. 6,600,220)

With respect to claims 22 and 23 Chu teaches the second semiconductor device (14b) is a memory modules however is silent in the external structure of the module. Barber teaches semiconductors item 62 in Fig. 5 see col. 8 lines 25-36 communicate power signals between each other in one operation and data signal in another. It would have been obvious to one of ordinary skill in the art at the time of the invention to communicate power from a first device in mode and from a second device in another mode in order to provide a reliable and redundant power signal to the chips to maintain operation.

With respect to claims 24 and 25 Chu as modified by Barber does not teach the second operating mode is a standby mode or refresh mode. It would have been obvious to one of ordinary skill in the art at the time of the invention to name the modes refresh or standby mode in order to distinguish between the different modes.

Barber teaches the communication of power signals and data signals across region 40 shown in Fig. 5, in a second configuration or mode, power may be supplied to processors (38) from the left side voltage converter when right side converter is not functioning properly such a mode and communication of power may considered a standby or a refresh mode as power is supplied from second or standby source, or alternately power refreshes the circuitry with power signal when the right side voltage converter is not supplying power.

With respect to claim 26 Chu does not teach the first operating mode is a working mode, in which external access to the second semiconductor device is performed. Odisho teaches the components are pluggable memory modules. It would have been

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obvious to one of ordinary skill in the art at the time of the invention to provide external access to the semiconductor device in order to remove the module when the memory module is no longer needed.

Alternatively Claims 1, 8 are rejected under 35 U.S.C. 102(a) as being anticipated by Nishikawa et al. (JP 2002-333687) where (U.S. Pub. No. 2004/0094820) is used as an English translation.

With respect to claim 1 Nishikawa teaches a system (Fig. 2A or 2B) comprising first semiconductor device (for example 208e), and second semiconductor device (209e), wherein the first semiconductor device (for example 208e) comprises a voltage supply means (VDD1), characterized in that said voltage supply means of said first semiconductor device is connected (signal path 21p in Fig. 2A) to said second semiconductor device, so that said voltage supply means of said first semiconductor device can provide (see paragraph 0096) a supply voltage for said second semiconductor device.

With respect to claim 8 Nishikawa teaches the system comprising one further semiconductor devices (for example 207e).

Alternatively Claims 2-7, 9-11, 18-19, 22-25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa et al. (U.S. Pub. No. 2004/0094820)

With respect to claim 2 Nishikawa teaches said first semiconductor device and said second semiconductor device are arranged in the same block (circuit block item 2Ca). Nishikawa does not teach the circuitry is contained within a housing,

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semiconductor components are typically found a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the circuit block of Nishikawa into a housing if in fact such a housing is not utilized by Nishikawa in order to protect the semiconductor.

With respect to claim 3 Nishikawa teaches the first and second semiconductor devices are arranged in a stacked manner (see arrangement of components in Fig. 1 or 2 from top to bottom and left to right)

With respect to claims 4-7 Nishikawa is silent on the on the detailed nature of the components and whether said components are plug mountable, DIL, SMD or PGA. As Applicant admits in page 2 lines 24-31 of the disclosure semiconductors are usually incorporated in appropriate housings e.g. SMD, plug mountable, DIL, PGA etc... It would have been obvious to one of ordinary skill in the art at the time of the invention to connected semiconductors as appropriate to the housing in order to provide a simple and reliable connection to other connected semiconductors.

With respect to claim 9 Nishikawa teaches said one further semiconductor device is arranged in the same circuit block (2Ca), as the first and said second semiconductor devices (208e and 209e). Nishikawa does not teach the circuitry is contained within a housing, semiconductor components are typically found a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the circuit block of Nishikawa into a housing if in fact such a housing is not utilized by Nishikawa in order to protect the semiconductor.

With respect to claim 10 Nishikawa teaches the voltage supply means (VDD) of said first semiconductor device (208e) is additionally also connected (via path 21p) to said one or to said several further semiconductor device, so that said voltage supply means (VDD1) of said first semiconductor device can additionally provide a supply voltage for said one or said several further semiconductor device (see paragraph 0096).

With respect to claim 11 Nishikawa teaches first semiconductor device (208e) comprises a further voltage supply means (VDD2) that is connected to said one or said several further semiconductor device, so that said further voltage supply means of said first semiconductor device (208e) can provide a supply voltage for said one or said several further semiconductor device (see paragraph 0096 or Fig. 2A).

With respect to claim 18 Nishikawa teaches the voltage supply means (VDD) provide a voltage supply for said first semiconductor device (208e).

With respect to claim 19 Nishikawa teaches the voltage supply means generates the respective supply voltage from an external voltage (supplied to the VDD terminal or pad).

With respect to claims 22 and 23 Nishikawa teaches the second semiconductor device (209e) comprises a voltage supply means (VDD2), and wherein, in a first operating mode (voltage supplied from VDD2) of said second semiconductor device, said voltage supply means (VDD2) of said second semiconductor device (209e) provides the supply voltage for said second semiconductor device (209e), and wherein, in a second operating mode (voltage supplied from VDD1) of said second

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semiconductor device, said voltage supply means (VDD1) of said first semiconductor device (208e) provides the supply voltage for said second semiconductor device.

With respect to claims 24 and 25 Nishikawa does not teach the second operating mode is a standby mode or refresh mode. It would have been obvious to one of ordinary skill in the art at the time of the invention to name the modes refresh or standby mode in order to distinguish between the different modes.

With respect to claim 27 Nishikawa teaches a device function adjusting means (see paragraph 0094-0095 where Nishikawa describes the stepping down of voltage), in particular an appropriate fuse (bonding wire connecting components item 208e and 209e), is provided on said first semiconductor device (208e), by means of which it is determined whether the corresponding semiconductor device is to assume the function of said first semiconductor device.

With respect to claim 28 Nishikawa teaches the voltage supply means (VDD) of said first semiconductor device (208e) is connected to a corresponding pad (see in Fig. 2) of said first semiconductor device (208e).

With respect to claim 29 Nishikawa teaches the pad of said first semiconductor device is connected to a corresponding pad of said second semiconductor device, which said voltage supply means of said second semiconductor device can be connected to (see Fig. 2).

With respect to claim 30 Nishikawa teaches the pad of said first semiconductor device is connected directly to the corresponding pad of said second semiconductor device by means of an appropriate bonding wire (see Fig. 2).

With respect to claim 31 Nishikawa teaches the pad of said first semiconductor device is connected indirectly to the corresponding pad of said second semiconductor device. Nishikawa does not teach the use of an interposer, however the interconnection seen in Fig. 1 between circuit blocks. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an interposer or other connection means to connect the circuit blocks in order to provide a reliable connection between circuit blocks.

Alternatively Claims 12-17, 20-21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa et al. (U.S. Pub. No. 2004/0094820) in view of Odisho et al. (U.S. Pat. No. 5,758,100)

With respect to claim 12-14 Nishikawa is silent on the on the detailed nature of the components specifically whether the first semiconductor device is a memory device. Odisho teaches a typical semiconductor integrated circuit (item 202) comprising a memory device (RAM module item 212). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semiconductor voltage supply configuration of Nishikawa with memory devices as seen in Odisho in order to supply memory modules with variable voltage requirements.

With respect to claim 15 Nishikawa as modified by Odisho are silent on whether the RAM is DRAM (dynamic RAM) as understood by the examiner the RAM modules are DRAM modules, while not explicitly stated by Odisho, however should one content otherwise, It would have been obvious to one of ordinary skill in the art at the time of the

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invention to use DRAM modules in order to supply typical memory modules is a computer with voltage.

With respect to claim 16 Odisho teaches the memory devices items 212 and additional circuitry may comprise a graphics card or a network card (col. 2 line 55) known to one of ordinary skill in the art to utilize ROM.

With respect to claim 17 Nishikawa as modified by Odisho teaches said memory device is a functional memory device or fundamental memory devices, respectively, in particular PLDs and/or PLAs as the memory devices of Odisho are controlled by a memory address bus and made up of transistors.

With respect to claims 20 and 21 Nishikawa teaches the voltage supply means (VDD) comprise a voltage regulating means and charge pump to control the voltage to memory modules with different voltage requirements.

With respect to claim 26 Nishikawa does not teach the first operating mode is a working mode, in which external access to the second semiconductor device is performed. Odisho teaches the components are pluggable memory modules. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide external access to the semiconductor device in order to remove the module when the memory module is no longer needed.

Conclusion


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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW



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